IN THE CLAIMS

1. (Original) A metal-oxide-semiconductor field effect transistor (MOSFET) device comprising:

a channel region formed on a monocrystalline silicon layer of a silicon–on-insulator (SOI) substrate;

a source/drain region formed in the monocrystalline silicon layer and comprising a deep junction region and a shallow extension region;

a first silicon oxide film pattern formed on the monocrystalline silicon layer to contact the deep junction region and doped with a first impurity of a first conductivity type at a first concentration;

a second silicon oxide film spacer formed on the monocrystalline silicon layer to contact the shallow extension region and doped with a second impurity of the first conductivity type at a second concentration;

a gate electrode formed on the channel region and having a T-shaped section; and

a gate dielectric film interposed between the channel region and the gate electrode.

2. (Original) The MOSFET device of claim 1, wherein the second silicon oxide film spacer contacts a sidewall of the first silicon oxide film pattern.

3. (Original) The MOSFET device of claim 1, wherein the second silicon oxide film spacer has an outer wall defining the length of the channel region.

4. (Original) The MOSFET device of claim 1, wherein the gate electrode is formed on the first silicon oxide film pattern and the second silicon oxide film spacer.

5. (Original) The MOSFET device of claim 1, wherein the first concentration is higher than the second concentration.

6. (Original) The MOSFET device of claim 1, wherein the first impurity and the second impurity are different from each other.

7. (Original) The MOSFET device of claim 6, wherein the first impurity is phosphorus(P) and the second impurity is arsenic (As).

8. (Original) The MOSFET device of claim 1, wherein the gate dielectric film is extended to between the first silicon oxide film pattern and the gate electrode and between the second silicon oxide film spacer and the gate electrode.

9. (Withdrawn) A method of manufacturing an MOSFET device, which comprises:

forming a first silicon oxide film pattern doped with a first impurity of a first conductivity type at a first concentration on an SOI substrate having a monocrystalline silicon layer thereon, the first silicon oxide film pattern having a hole through which a portion of the monocrystalline silicon layer is exposed;

forming a second silicon oxide film spacer doped with a second impurity of the first conductivity type at a second concentration on a sidewall of the first silicon oxide film pattern;

diffusing the first impurity of the first silicon oxide film pattern and the second impurity of the second silicon oxide film spacer onto the monocrystalline silicon layer to form a source/drain region comprising a deep junction region and a shallow extension region;

forming a gate dielectric film on the exposed portion of the monocrystalline silicon layer; and

forming a gate electrode with a T-shaped section on the gate dielectric film

10. (Withdrawn) The method of claim 9, wherein the second silicon oxide film spacer is doped with the second impurity at a lower concentration than the first impurity of the first silicon oxide film pattern.

11. (Withdrawn) The method of claim 9, wherein the step of forming the second silicon oxide film spacer comprises:

forming a second silicon oxide film doped with the second impurity at the second concentration on the upper surface and sidewall of the first silicon oxide film pattern and the exposed portion of the monocrystalline silicon layer; and

removing portions of the second silicon oxide film by dry etching so that the second silicon oxide film spacer remains.

12. (Withdrawn) The method of claim 9, wherein in the formation of the source/drain region, the first silicon oxide film pattern and the second silicon oxide film spacer are subjected to rapid thermal process to diffuse the first impurity and the second impurity.

13. (Withdrawn) The method of claim 9, wherein the gate dielectric film is extended to the exposed portion of the monocrystalline silicon layer and the upper surfaces of the second silicon oxide film spacer and the first silicon oxide film pattern.

14. (Withdrawn) The method of claim 9, further comprising doping the exposed portion of the monocrystalline silicon layer with an impurity of the second conductivity type, which is an opposite type to the first conductivity type, to form an ion implantation region for adjusting a threshold voltage, after the formation of the first silicon oxide film pattern.

15. (Withdrawn) The method of claim 14, wherein in the formation of the ion implantation region for adjusting the threshold voltage, the impurity of the second conductivity type is implanted using a photoresist pattern formed on the first silicon oxide film pattern as an ion implantation mask.